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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,186	01/14/2004	Jimmies Earl DeWitt JR.	AUS920030540US1	4157

35525 7590 05/18/2006

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EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 05/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,186	DEWITT ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/10/06, 1/30/06, 2/14/06, 4/25/06*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 4/25/06 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. The record on file does not include the three non-patent literatures listed on the IDS.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6, 8-12, and 16-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Levine et al. (U.S. Patent No. 5,691,920)

Referring to claim 1: Levine discloses a performance-monitoring unit (Abstract) and one or more hardware counters (column 10, lines 58-59) located within the performance-monitoring unit (figure 4, structures 50 and 51). Levine discloses a variety of operations of the performance-monitoring unit (column 10, lines 34-56); Levine discloses setting the performance-monitoring unit to selectively monitor the instructions within specific addresses (column 12, 2nd paragraph).

The instructions within specific addresses are a selected interrupt handling routine, and the Levine's selective monitoring on the particular instructions is the claimed hardware counters' counting the occurrence of events during an interrupt of a selected type. Furthermore, Levine disclosed two separate counters for selected events (figure 6A, column 8, lines 57-60). Hence, the claim is anticipated by Levine.

Referring to claims 2-3: Since the nature of an interrupt process comprises of an interrupt request, interrupt request acceptance, passing the control to the interrupt handler, and interrupt service routine; thus, any events been monitored during the interrupt is during a state of the interrupt.

Referring to claim 4: Levine discloses monitoring instruction execution and storage control (column 1, lines 65), which are the claimed multiple types of events.

Referring to claim 5: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Referring to claim 6: Levine discloses clock cycles (column 1, lines 66-67) and cache misses (column 14, line 9).

Referring to claims 8-10: The rejections for the claims 1-3 apply; furthermore, Levine discloses that to effectively evaluate the flow of the instructions through the processor's pipeline, all stages are *preferably* examined simultaneously (column 14, lines 63-65). Since Levine discloses that it is preferred to examine all stages, Levine implicitly discloses counting at least one event for either a selected state of the interrupt or each state of the interrupt.

Referring to claim 11: Levine discloses clock cycles (column 1, lines 66-67) and cache misses (column 14, line 9).

Referring to claim 12: Levine discloses monitoring multiple types of events during the stall, which is the claimed counting multiple types of events for the same state.

Referring to claim 13: Levine discloses one or more hardware counters (column 10, lines 58-59).

Referring to claim 14: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, and the instructions within specific addresses are a selected interrupt handling routine, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Referring to claim 16: The rejections for the claims 1-3 apply; furthermore, Levine discloses that to effectively evaluate the flow of the instructions through the processor's pipeline, all stages are *preferably* examined simultaneously (column 14, lines 63-65). Since Levine discloses that it is preferred to examine all stages, Levine discloses counting at least one event for either a selected state of the interrupt or each state of the interrupt.

Referring to claim 17: The nature of an interrupt process comprises of an interrupt request, interrupt request acceptance, passing the control to the interrupt handler, and interrupt service routine.

Referring to claim 18: Levine discloses clock cycles (column 1, lines 66-67) and cache misses (column 14, line 9).

Referring to claim 19: Levine discloses monitoring multiple types of events during the stall, which is the claimed counting multiple types of events for the same state.

Referring to claim 20: Levine discloses one or more hardware counters (column 10, lines 58-59).

Referring to claim 21: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, and the instructions within specific addresses are a selected interrupt handling routine, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-6, 8-14, and 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Levine.

Referring to claim 1: The admitted prior art discloses a performance-monitoring unit (Specification, page 3, last paragraph, line 6) and one or more hardware counters (Specification, page 3, last paragraph, lines 1-2) located within the performance-monitoring unit. The admitted prior art does not disclose that the one or more hardware counters count the occurrence of events during an interrupt of a selected type.

Levine discloses a variety of operations of the performance-monitoring unit (column 10, lines 34-39); Levine discloses setting the performance-monitoring unit to selectively monitor the instructions within specific addresses (column 12, 2nd paragraph). The instructions within specific addresses are a selected interrupt handling routine, and the Levine's selective monitoring on the particular instructions is the claimed hardware counters' counting the occurrence of events during an interrupt of a selected type. Levine teaches one to analyze the system performance and to focus particular sets of instructions for examining the performance bottleneck. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Levine's teaching onto the admitted prior art because Levine teaches one to analyze the system performance and to focus particular sets of instructions for examining the performance bottleneck.

Referring to claim 2: Since an interrupt process comprises of an interrupt request, interrupt request acceptance, passing the control to the interrupt handler, and interrupt service routine (Specification, page 4, 2nd paragraph, lines 3-11); thus, any events been monitored during the interrupt is during a state of the interrupt.

Referring to claim 3: The admitted prior art discloses that the interrupt includes states of accepting the signal, invoking an interrupt handler routine of the interrupt, completion of the interrupt handler routine, and interrupt return (Specification, page 4, 2nd paragraph, lines 3-11).

Referring to claim 4: The admitted prior art discloses monitoring multiple types of events (Specification, page 3, last paragraph, lines 3-4, page 4, 1st paragraph, lines 5-7).

Referring to claim 5: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Referring to claim 6: The admitted prior art discloses counting clock cycles and cache misses (Specification, page 3, last paragraph, lines 3-4).

Referring to claims 8-9: The rejections for the claims 1-3 apply; the admitted prior art does not explicitly discloses counting at least one event for either a selected state of the interrupt or each state of the interrupt. Levine discloses that to effectively evaluate the flow of the instructions through the processor's pipeline, all stages are *preferably* examined simultaneously (column 14, lines 63-65). Levine's examination on all stages are the claimed counting at least one event for either a selected state of the interrupt or each state of the interrupt. Levine teaches one on how to locate the performance bottleneck by tracing the processing through all stages.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Levine's teaching onto the admitted prior art because Levine teaches one on how to locate the performance bottleneck for improve the system performance.

Referring to claim 10: The admitted prior art discloses that the interrupt includes states of accepting the signal, invoking an interrupt handler routine of the interrupt, completion of the interrupt handler routine, and interrupt return (Specification, page 4, 2nd paragraph, lines 3-11).

Referring to claim 11: The admitted prior art discloses counting clock cycles and cache misses (Specification, page 3, last paragraph, lines 3-4).

Referring to claim 12: Levine discloses monitoring multiple types of events during the stall, which is the claimed counting multiple types of events for the same state.

Referring to claim 13: The admitted prior art discloses one or more hardware counters (Specification, page 3, last paragraph, lines 1-2).

Referring to claim 14: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Referring to claim 16: The rejections for the claims 1-3 apply; the admitted prior art does not explicitly discloses counting at least one event for either a selected state of the interrupt or each state of the interrupt. Levine discloses that to effectively evaluate the flow of the instructions through the processor's pipeline, all stages are *preferably* examined simultaneously (column 14, lines 63-65). Levine's examination on all stages are the claimed counting at least one event for either a selected state of the interrupt or each state of the interrupt. Levine teaches one on how to locate the performance bottleneck by tracing the processing through all stages.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Levine's teaching onto the admitted prior art because

Levine teaches one on how to locate the performance bottleneck for improve the system performance.

Referring to claim 17: The admitted prior art discloses that the interrupt includes states of accepting the signal, invoking an interrupt handler routine of the interrupt, completion of the interrupt handler routine, and interrupt return (Specification, page 4, 2nd paragraph, lines 3-11).

Referring to claim 18: The admitted prior art discloses counting clock cycles and cache misses (Specification, page 3, last paragraph, lines 3-4).

Referring to claim 19: Levine discloses monitoring multiple types of events during the stall, which is the claimed counting multiple types of events for the same state.

Referring to claim 20: The admitted prior art discloses one or more hardware counters (Specification, page 3, last paragraph, lines 1-2).

Referring to claim 21: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

7. Claims 7, 15, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Levine in view of previously cited "Computer System Architecture" by Morris Mano or as being unpatentable over the admitted prior art in view of Levine and Mano.

Referring to claims 7, 15, and 22: The disclosures of the admitted prior art and Levine are stated above. As stated above, Levine discloses monitoring the particular interrupt according to the instructions address, and Levine discloses two separate counters for event selections (figure

6A, column 8, lines 57-60); thus, Levine discloses the hardware counters counting events separately. But neither explicitly discloses a second interrupt interrupts a first interrupt.

Mano, as a popular academic textbook, discloses managing interrupt according to its priority (pages 434-435). Mano discloses that a higher priority interrupt can interrupt an in-process lower priority interrupt (page 435, 2nd paragraph). Mano teaches one to manage the limited system resources by prioritizing interrupt. Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Mano's teaching onto the admitted prior art and Levine because Mano teaches one to manage the limited system resources by prioritizing interrupt.

Response to Arguments

8. In response to Applicant's argument dated on 4/25/06: The Office Action has been revised above to replace the invalid prior art cited in the previous Office Action, and to further clarify the mapping to the claimed limitations as argued. Examiner hereby issues a second Non-Final Action.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-36283628. The examiner can normally be reached on max flex. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676 or on the central telephone number, (571) 272-2100. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests

to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
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Justin King
May 6, 2006